BCT100N10P

Silicon N-Channel MOSFET

Features

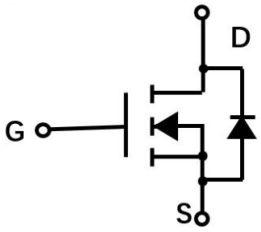
- 100V, 68A
- $R_{DS(ON)}$ = 9.5mΩ (Max.) @ V_{GS} = 10V, I_D = 20A
- Low $R_{DS(on)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- 100% UIS tested , 100% △VDS Tested
- RoHS and Halogen-Free Compliant

Package

TO-220F

Application

- High Frequency Switching
- Synchronous Rectification



Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		100	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current note5	T_C = 25℃	68	A
I_D	Continuous Drain Current note5	T_C = 100℃	42.5	A
I_{DM}	Pulsed Drain Current note3		268	A
P_D	Power Dissipation note2	T_C = 25℃	78	W
I_{AS}	Avalanche Current note3,6		18	A
E_{AS}	Single Pulse Avalanche Energy note3,6		81	mJ
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.6	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient note1,4		50	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	100	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 80V, V_{GS} = 0V	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.2	1.8	2.6	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 20A	-	8.2	9.5	mΩ
		V_{GS} = 4.5V, I_D = 10A	-	11.3	13.5	mΩ
g_{fs}	Forward Threshold Voltage	V_{DS}= 5V, I_D= 20A	-	15.9	-	S
R_g	Gate Resistance	V_{DS} = V_{GS}=0V, f = 1.0MHz	-	1.62	-	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1.0MHz	-	2018	-	pF
C_{oss}	Output Capacitance		-	580	-	pF
C_{rss}	Reverse Transfer Capacitance		-	28	-	pF
Switching Characteristics						
Q_g	Total Gate Charge	V_{DS}= 50V, I_D = 20A, V_{GS} = 10V	-	38.5	-	nC
Q_{gs}	Gate-Source Charge		-	8	-	
Q_{gd}	Gate-Drain(“Miller”) Charge		-	9	-	
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 50V, I_D = 20A, R_G = 3Ω, V_{GS}=10V	-	17	-	ns
t_r	Turn-On Rise Time		-	4	-	
$t_{d(off)}$	Turn-Off Delay Time		-	32	-	
t_f	Turn-Off Fall Time		-	8	-	
Diode Characteristics						
I_S	Continuous Source Current		-	-	68	A
V_{SD}	Diode Forward Voltage	I_S=20A . V_{GS} = 0V	-	0.88	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD}=20A, dI_{SD}/dt=100A/μs	-	50.4	-	ns
Q_{rr}	Reverse Recovery Charge		-	68	-	nC

Notes:

1. The value of $R_{\theta JC}$ is measured in a still air environment with TA =25°C and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

2. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

3. Single pulse width limited by junction temperature $T_{J(MAX)}$=150°C.

4. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

5. The maximum current rating is package limited.

6. The EAS data shows Max. rating. The test condition is V_{DS}=50V,V_{GS}=10V,L=0.5mH

Typical Performance Characteristics

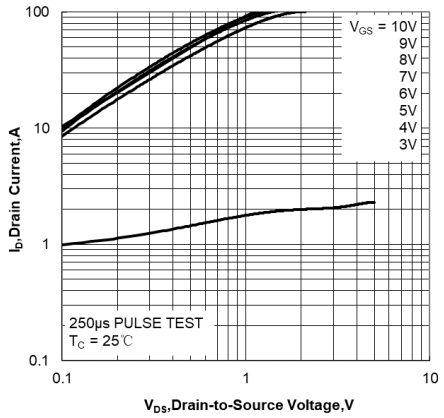


Figure 1. Output Characteristics

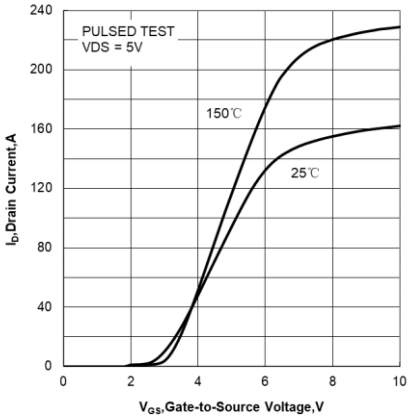


Figure 2. Transfer Characteristics

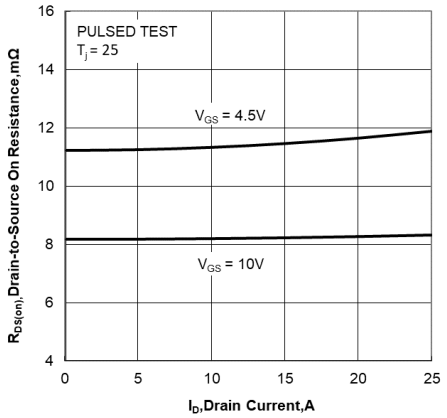


Figure 3. Drain-to-Source On Resistance vs Drain Current

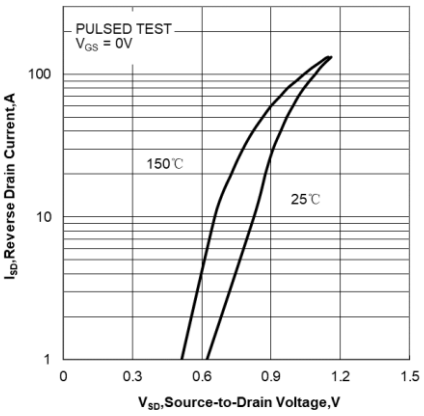


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

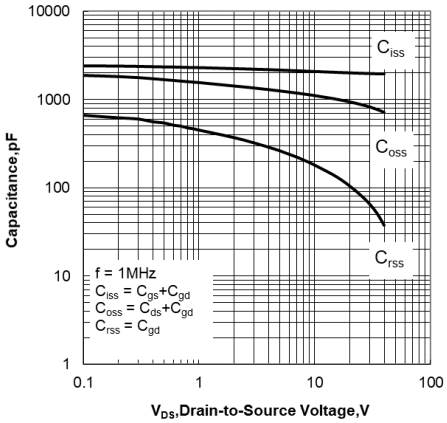


Figure 5. Capacitance Characteristics

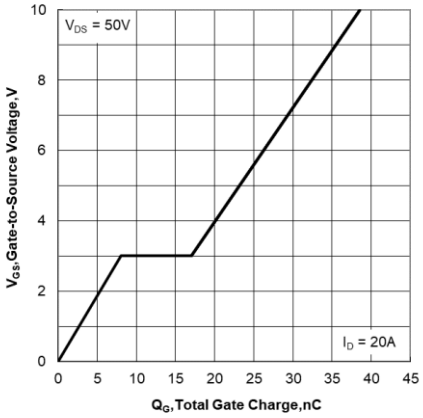


Figure 6. Gate Charge Characteristics

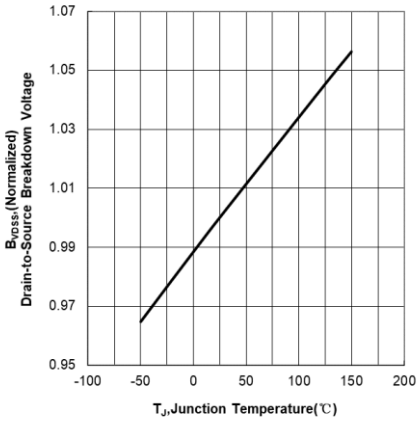


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

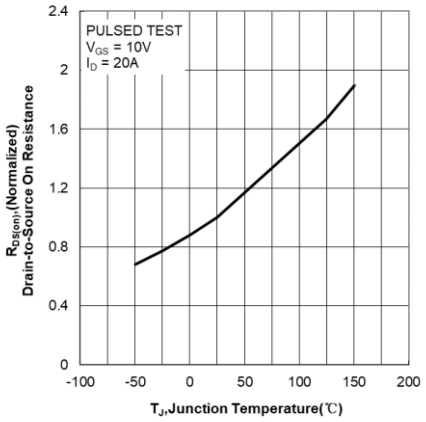


Figure 8. Normalized On Resistance vs Junction Temperature

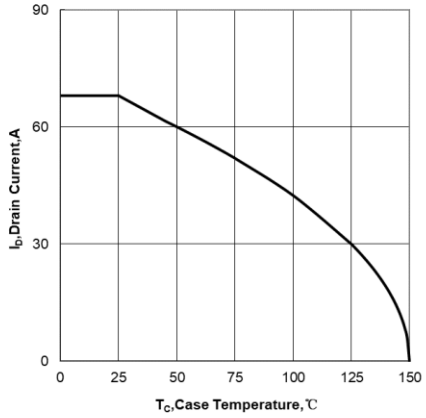


Figure 9. Maximum Continuous Drain Current vs Case Temperature

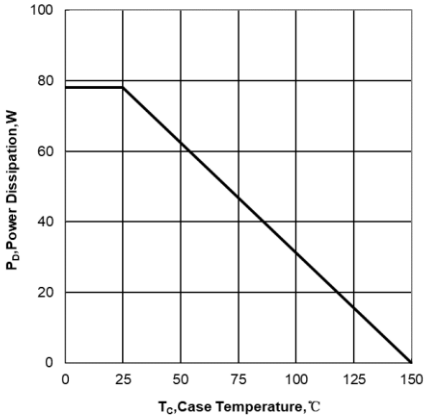


Figure 10. Maximum Power Dissipation vs Case Temperature

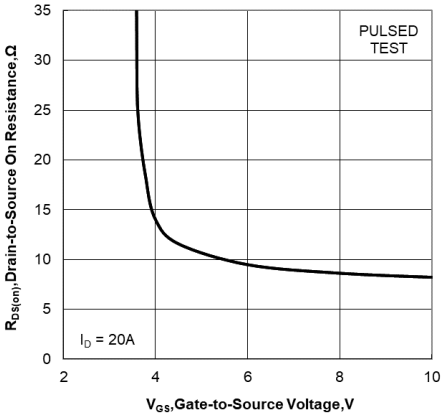


Figure11. Drain-to-Source On Resistance vs Gate Voltage and Drain Current

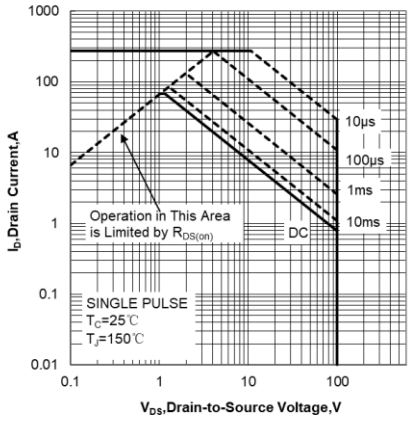


Figure 12. Maximum Safe Operating Area

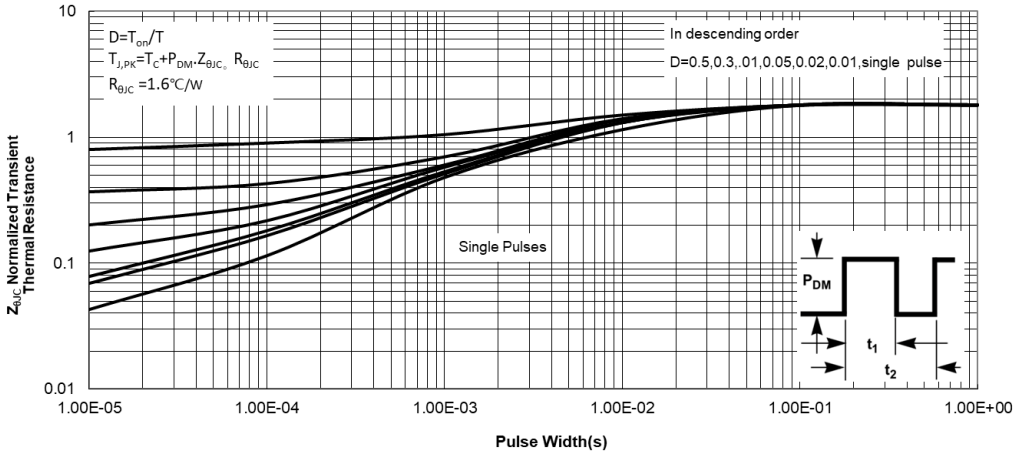


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case